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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,611	09/18/2003	KokHoe Chia	STL11343	4044

7590 12/19/2006

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EXAMINER	
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ART UNIT	PAPER NUMBER
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
2 MONTHS	12/19/2006	PAPER

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/664,611
Filing Date: September 18, 2003
Appellant(s): CHIA ET AL.

John D. Veldhuis-Kroeze
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 27 September 2006 appealing from the Office action mailed 4 April 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US Patent 6,336,202 B1 Tsuchimoto et al. 01-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuchimoto et al., US Patent 6,336,202 B1 (hereinafter Tsuchimoto).

As for claim 15, Tsuchimoto teaches a method of managing a buffer random access memory, the buffer random access memory having a first portion allocated for a defect table and a second portion allocated for data caching, (referring to Fig. 1, the controller (element 5) comprises a buffer RAM (element 14). The RAM is allocated to the system for two purposes, including; a defect table (col. 3, lines 38-50 – the controller reads the defect map (table) from a disk and writes it to the RAM), and

the remaining section is used for data caching (col. 3, lines 18-28 – data to be written or read is cached in the RAM). Note the RAM is allocated for these purposes, however a determination of exactly how much memory is used for each is not determined until the defect map is actually written from the disk to the RAM. In other words, the preamble does not require some sort of statically assigned or allocated "first" and "second" portions. The very fact that the memory is used for these two purposes is "allocation" based on Examiner's broadest reasonable interpretation of the claims, consistent with Appellant's original specification – see MPEP § 2111) – also note the preamble corresponds to Examiner's illustration per Fig. 1A, *infra*, the method comprising:

determining actual memory space of the first portion of the buffer random access memory occupied by the defect table to identify unused memory space of the first portion (col. 3 lines 18-25 and 38-50 demonstrate how the RAM is used for both the defect table and data caching. The controller as illustrated in Fig. 1 must inherently make a determination which data in the RAM is the defect table, and which area in the RAM is for data caching in order for Tsuchimoto's system to work. In other words, the system can determine which area/s of the memory will be used for caching, and which cannot (i.e. memory used for defect table) once the table is written) – this step corresponds to Examiner's illustration per Fig. 1B, *infra*; and

reallocating the unused memory space of the first portion of the buffer random access memory for use in data caching (the remaining memory area in the RAM, not being used to store the variable sized defect table can now be used (i.e.

reallocated) for data caching purposes. Referring to col. 5, lines 57-67, Tsuchimoto aims at minimizing the size of the defect map so that it occupies a minimal amount of the RAM in the controller. The remaining area of the RAM is now allocated for data caching purposes as described in col. 3, lines 18-25). Col. 5, lines 15-20 additionally support this assertion – i.e. the capacity needed to record the table within the RAM is minimized using a variable length table. In other words, a greater amount of memory may be assigned to cache data once the table size is determined and minimized. Note this step corresponds to Examiner's illustration per Fig. 1C, *infra*.

Additionally, it is worthy to note that Tsuchimoto teaches the use of a reassign table in col. 6, lines 43-65. This reassign table (which is also referred to as the defect map) can be produced either before *or after* (emphasis added) logical formatting. In other words, an original defect map can be produced, and then subsequently updated to account of any change in the sectors that are identified during use of the disk drive unit. Any changes that are required recorded in the reassign table, which can be written to the RAM at a later time. Please refer to col. 7, lines 6-26. In other words, the table may be originally created, and then subsequently updated to provide address information on sectors that fail or become defective after LBAs are assigned. The table is modified, hence the amount of memory required to store the information will change (recall the table is of variable length), resulting in a change in amount of memory remaining in the RAM for caching purposes. When the table is rewritten, the system will "reallocate" memory in the RAM based on the determination of how much memory is available within the RAM, to maximize remaining memory for caching.

As for claims 16-17 Tsuchimoto teaches a disk drive unit (i.e. mass storage device) comprising a controller (element 5), which controls an MPU (element 12) and an HDC (element 11), used to execute control over the data storage system (col. 3, lines 18-25).

(10) Response to Argument

Appellant's arguments have been fully considered but they are not persuasive. As for claim 15, Appellant alleges two deficiencies within the cited prior art including:

i. "The Step of Determining Actual Memory Space is Not Anticipated" (refer to pages 6 through 7 of the Appellant's brief) and

ii. "The Step of Reallocating the Unused Memory Space is Not Anticipated" (refer to pages 7 through 9 of the Appellant's brief)

Under the heading, i. "The Step of Determining Actual Memory Space is Not Anticipated", Appellant contends "there is no teaching by Tsuchimoto to conclude that the system disclosed by that reference operates any differently than in this conventional manner [i.e. the defect table is fixed across all disc drives of a particular type]". Appellant further concedes that Tsuchimoto teaches a RAM allocated for data caching and allocated for caching, however further alleges that Tsuchimoto's system would not inherently determine actual memory space of the first portion which is actually occupied by the defect table to identify unused memory space of the first potion.

Examiner maintains however that Tsuchimoto's system must inherently determine which area/s of the memory is being occupied by the table (once written from the disk) in order for the remainder of the memory to be used as a cache as described in col. 3, lines 18-25 of his disclosure. More specifically, the preamble of the claim requires "a first portion allocated for a defect table" and "a second portion allocated for data caching". Tsuchimoto is in fact permitting the memory to be used for two purposes (i.e. for storing the table, and caching), hence some portion of the memory is "allocated" to each (though the precise assignment of memory for each purpose has yet to be determined). This point is illustrated in Fig. 1 provided *infra*. Fig. 1A illustrates Tsuchimoto's RAM (Fig.1, element 14) prior to writing the defect table to the RAM. At this point, the RAM is to be used for caching and a defect table (i.e. reserved or allocated for these purposes), however the actual memory space they will each respectively occupy has not yet been definitively determined. The very fact that the memory is used for these two purposes is "allocation" based on Examiner's broadest reasonable interpretation of the claims, consistent with Appellant's original specification. The variable length table is aimed at minimizing the amount of memory used by the table (col. 5, lines 15-20), hence maximizing the amount of memory for caching purposes. The amount of memory space is determined once the table is written, which subsequently enables the system to determine what memory space remaining can be used for caching. Again by referring to Examiner's Fig. 1 (more specifically Fig. 1B, *infra*), the actual memory space in which the table occupies must be determined once it is written, else it would be overwritten once the system begins to cache data.

This argument is not persuasive per the reasons discussed *supra*.

Under the heading "The Step of Reallocating the Unused Memory Space is Not Anticipated", Appellant contends, "Tsuchimoto provides no actual teaching of reallocating unused memory space of the first portion of the random access memory for use in data caching". Appellant further alleges "even if the remaining memory area in the RAM, which is not being used to store the defect table can be used for data caching purposes... ; the mere fact that is can be used in this manner does not provide a teaching of such a reallocation use". Additionally, Appellant contends, "the fact that Tsuchimoto aims at minimizing the size of the defect map so that it occupies a minimal amount of RAM in the controller is not in and of itself a teaching of the recited reallocating limitation". Appellant sets forth a similar argument with respect to the cited reassign table as described by Tsuchimoto, stating "the fact that the table can be modified after logical formatting, changing the actual memory requirements of the table, does not in and of itself lead to the conclusion that RAM allocated for the table will be reallocated for use in data caching".

Examiner however maintains that Tsuchimoto's is in fact enabling a form of "reallocation" once the table is determined and written to the RAM. Once this step is performed, the system definitively assigns unused memory (unused by the table) for data caching purposes. Appellant alleges that just because the memory now can be used for caching, doesn't mean it will be (hence it is not reallocated) is not persuasive. The thrust Tsuchimoto's teaching of a variable length defect table is to minimize the memory needed to store it within the RAM (or conversely maximizing the amount of

memory available to the system for caching). In other words, Tsuchimoto aims to minimize the table explicitly for the purposes of freeing more memory to be used for other purposes (in this case caching, since that is in fact the primary function of the RAM). Referring again to Examiner's Fig. 1, *infra* (more specifically, Fig. 1C), once the table size is determined by being physically assigned within the RAM, the remaining memory can be cached (hence memory not used by the table is used for caching). Again, the aim of Tsuchimoto's teachings is to minimize the size of the table in order to create more memory for other purposes, in this case caching. Additionally (as per the rejection set forth *supra*), the variable length table can be created/modified either before or after logical formatting, hence changing the length of the table dynamically through operation, and changing the amount of memory required to store the table in the RAM – col. 6, lines 43-65 and col. 7, lines 6-26. Appellant's contention that "the memory allocated for the table in Tsuchimoto could be large enough to allow for changes to the defect table" is not persuasive as again, the thrust of Tsuchimoto's variable table aims to minimize the table size at the onset, and further minimize the size of the table based on any subsequent modifications to the table.

In summary, both arguments (i. and ii.) are not persuasive per the reasons discussed *supra*, and for the above reasons, it is believed that the rejections should be sustained.

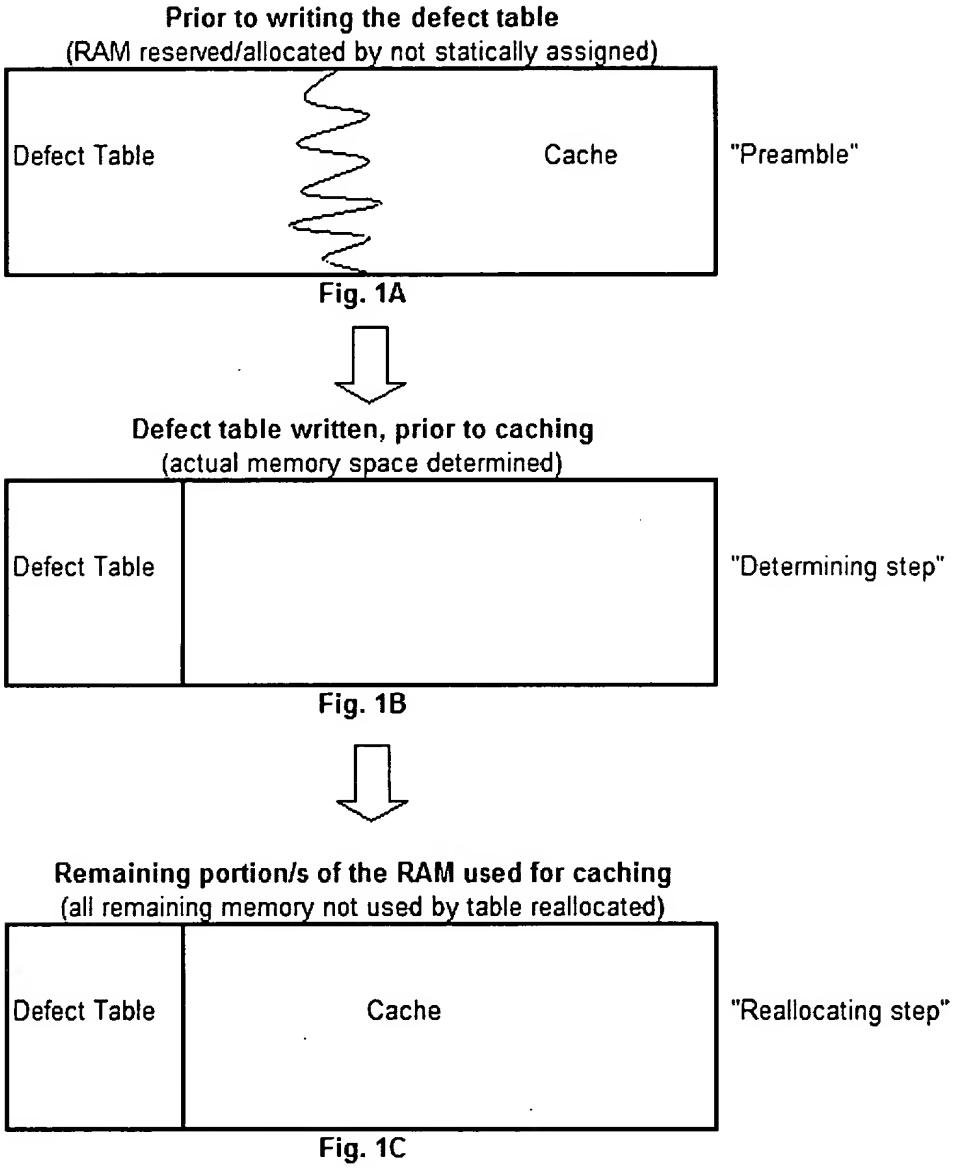

Fig. 1

*Note the outlined box as illustrated in each of these figures corresponded to Tsuchimoto's RAM (Fig.1, element 14)

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Respectfully submitted,

Craig E Walter

Examiner

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SUPERVISORY PATENT EXAMINER
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